

Remarks

Prior to entry of the present Amendment, claims 1-37 were pending in the present application. Claim 1 is amended above. Claims 4 and 26-37 are cancelled above without prejudice. No new matter is added by the claim amendments. Entry is respectfully requested.

The specification stands objected to for an informality. The title is amended above to state "METHOD OF FABRICATING A MOS TRANSISTOR WITH ELEVATED SOURCE/DRAIN STRUCTURE USING A SELECTIVE EPITAXIAL GROWTH PROCESS". Entry of the amendment and removal of the objection are respectfully requested.

Claims 1, 4, 8, 9, 12, 24 and 25 stand rejected under 35 U.S.C. 102(b) as being anticipated by Yu, *et al.* (U.S. Patent Number 6,187,642). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.* in view of Lin (U.S. Patent Number 6,727,543). Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.* in view of Chau, *et al.* (U.S. Patent Number 6,326,664). Claims 5-7, 11, 14, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.* Reconsideration of the rejections and allowance the claims are respectfully requested.

In the present invention as claimed in independent claim 1, a method of fabricating a metal-oxide semiconductor transistor having an elevated source/drain structure includes "following formation of" a "first gate spacer, forming a first epi-layer on the semiconductor substrate". The method further includes "ion-implanting a dopant in the first epi-layer and in the semiconductor substrate to form a source/drain extension region in the semiconductor substrate after forming the first epi-layer". The method further includes "following formation of the

source/drain extension region, forming a second gate spacer on lateral side surfaces of the first gate spacer”, and, “following formation of the second gate spacer, forming a second epi-layer on the first epi-layer”. The method further includes “ion implanting a dopant in the second epi-layer, in the first epi-layer and in the semiconductor substrate to form a deep source/drain region below the source/drain extension region in the semiconductor substrate after forming the second epi-layer”.

Yu, *et al.* discloses that a selective Si epitaxial growth process is used to grow first semiconductor layers 52 on the implant junctions 45, which are previously formed in the substrate 32. A dopant implantation 53 is then used to transform the first semiconductor layer 52 into raised source/drain extensions 54 with a bottom surface adjacent to the implant junctions 45. Second dielectric spacers 55 are formed adjacent first dielectric spacers 48. A selective Si epitaxial growth process is used to grow second semiconductor layers 58 on the top surface of the raised source/drain extensions 54, the second semiconductor layers 58 extending from the isolation trenches to the second dielectric spacers 55. A dopant implantation 60 is used to dope the second semiconductor layers 58 and a rapid thermal-anneal is used to transform the doped second semiconductor layers 58 into raised source/drain regions.

Yu, *et al.* fails to teach or suggest a method of fabricating a metal-oxide semiconductor transistor that includes “following formation of” a “second gate spacer, forming a second epi-layer on” a “first epi-layer”, and “ion implanting a dopant in the second epi-layer, in the first epi-layer and in” a “semiconductor substrate to form a deep source drain region below” a “source drain extension region in the semiconductor substrate”, as claimed in claim 1. Instead, in Yu, *et al.*, a dopant implantation 60 is used to dope the second semiconductor layers 58, so that raised

source/drain regions 54 can be formed. Yu, *et al.* does not teach formation of a “deep source/drain region below the source drain extension region in the semiconductor substrate” after “forming the second epi-layer”, as claimed in claim 1.

Reconsideration and removal of the rejection of claim 1 under 35 U.S.C. 102(e) as being anticipated by Yu, *et al.* are therefore respectfully requested. With regard to the dependent claims 4, 8, 9, 12, 24 and 25, it follows that these claims should inherit the allowability of the independent claim 1 from which they depend. Further with regard to the rejection of claims 5-7, 10, 11 and 13-23 under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.*, it follows that these claims should inherit the allowability of independent claim 1 from which they depend.

With regard to the rejection of claim 2 under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.* and Lin, Lin is cited in the Office Action as disclosing forming a first gate oxide 230 on the lateral side surfaces of the gate electrode 210 before the first gate spacer 240 is formed, and forming a second gate oxide 250 on the lateral side surfaces of the first gate spacer before the second gate spacer 260 is formed. Lin fails to teach or suggest a method of fabricating a metal-oxide semiconductor transistor that includes “following formation of” a “second gate spacer, forming a second epi-layer on” a “first epi-layer”, and “ion implanting a dopant in the second epi-layer, in the first epi-layer and in” a “semiconductor substrate to form a deep source drain region below” a “source drain extension region in the semiconductor substrate”, as claimed in claim 2. Accordingly, it is submitted that the combination of Yu, *et al.*, as discussed above, and Lin fails to teach or suggest the invention as claimed in claim 2. Reconsideration of the rejection of, and allowance of, claim 2 is respectfully requested.

With regard to the rejection of claim 3 under 35 U.S.C. 103(a) as being unpatentable over Yu, *et al.* and Chau, *et al.*, Chau, *et al.* is cited in the Office Action as disclosing a method of fabricating a transistor 40 that comprises forming a semiconductor material 314 on the gate electrode 306 and in recesses 312, an ion implantation step for forming source/drain contact region 322, and forming silicide 320 on the semiconductor material 314 after formation of the source/drain contact region 322. Chau, *et al.*, like Yu, *et al.*, fails to teach or suggest a method of fabricating a metal-oxide semiconductor transistor that includes “following formation of” a “second gate spacer, forming a second epi-layer on” a “first epi-layer”, and “ion implanting a dopant in the second epi-layer, in the first epi-layer and in” a “semiconductor substrate to form a deep source drain region below” a “source drain extension region in the semiconductor substrate after forming the second epi-layer”, as claimed in claim 3. Accordingly, it is submitted that the combination of Yu, *et al.* and Chau, *et al.* fails to teach or suggest the invention as claimed in claim 3. Reconsideration of the rejection of, and allowance of, claim 3 is respectfully requested.

Closing Remarks

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

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